AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Apparatus for simulating data processing operations performed by a data processing apparatus, said apparatus comprising:

a hardware simulator responsive to one or more stimulus signals to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus;

a plurality of signal interface controllers coupled to said hardware simulator, each signal interface controller serving to perform one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said hardware simulator and said signal interface controller as part of simulating said data processing operations; ~~and~~

a test scenario manager coupled to said plurality of signal interface controllers and operable to transfer test scenario controlling messages to said plurality of signal interface controllers, at least one of said test scenario controlling messages including:

(i) data defining a simulation action to be performed by a signal interface controller; and

(ii) data defining when said signal interface controller should perform said simulated action~~,~~; and

a time generator coupled to said plurality of signal interface controllers and said test scenario manager for generating messages specifying time defining events corresponding to advancement of simulated time for said hardware simulator.

wherein said test scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager via said shared data memory independently of advancement of simulated time by said messages specifying time defining events, said data being readable from said shared data memory by another signal interface controller.

2. (Original) Apparatus as claimed in claim 1, wherein said data defining when said signal interface controller should perform said simulated action includes at least one of:

(i) a time value;

(ii) a delay value; and

(iii) a value specifying said simulated action should be performed when a specified event is simulated as occurring.

3. (Canceled).

4. (Previously Presented) Apparatus as claimed in claim 1, wherein a first signal interface controller is responsive to simulation results captured by a second signal interface controller, written to said shared data memory by said second signal interface controller and then read from said shared data memory by said first signal interface controller.

5. (Original) Apparatus as claimed in claim 1, wherein said hardware simulation is simulated using software running upon a general purpose computer.

6. (Original) Apparatus as claimed in claim 1, wherein each signal interface controller includes an action queue of simulation actions to be performed by said signal interface controller.

7. (Original) Apparatus as claimed in claim 6, wherein each signal interface controller includes a test scenario manager interface operable to exchange test scenario controlling messages with said test scenario manager and to add simulation actions to said action queue.

8. (Original) Apparatus as claimed in claim 6, wherein each signal interface controller includes a peripheral interface operable to transform simulation actions specified in said action queue into signal values exchanged with said hardware simulation.

9. (Original) Apparatus as claimed in claim 1, wherein test scenario manager sends a machine generated sequence of simulation actions to said plurality of signal interface controllers to perform random simulation testing of said data processing apparatus.

10. (Original) Apparatus as claimed in claim 1, wherein said test scenario manager is operable as a master device and said plurality of signal interface controllers are operable as slave devices to said master device.

11. (Currently Amended) A method of simulating data processing operations performed by a data processing apparatus, said method comprising the steps of:

in response to one or more stimulus signals, using a hardware simulator to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus;

performing in each of a plurality of signal interface controllers coupled to said hardware simulator one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said hardware simulator and said signal interface controller as part of simulating said data processing operations; and

transferring test scenario controlling messages from a test scenario manager to said plurality of signal interface controllers, at least one of said test scenario controlling messages including:

(i) data defining a simulation action to be performed by a signal interface controller; and

(ii) data defining when said signal interface controller should perform said simulated action~~;~~; and

generating messages specifying time defining events corresponding to advancement of simulated time for said hardware simulator,

wherein said test scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager, said data being readable from said shared data memory by another signal interface controller.

whereby said test scenario controlling messages are communicated via said shared data memory independently of advancement of simulated time by said messages specifying time defining events.

12. (Original) A method as claimed in claim 11, wherein said data defining when said signal interface controller should perform said simulated action includes at least one of:

(i) a time value;

(ii) a delay value; and

(iii) a value specifying said simulated action should be performed when a specified event is simulated as occurring.

13. (Canceled).

14. (Previously Presented) A method as claimed in claim 11, wherein a first signal interface controller is responsive to simulation results captured by a second signal interface controller, written to said shared data memory by said second signal interface controller and then read from said shared data memory by said first signal interface controller.

15. (Original) A method as claimed in claim 11, wherein said hardware simulation is simulated using software running upon a general purpose computer.

16. (Original) A method as claimed in claim 11, wherein each signal interface controller includes an action queue of simulation actions to be performed by said signal interface controller.

17. (Original) A method as claimed in claim 16, wherein each signal interface controller includes a test scenario manager interface operable to exchange test scenario controlling messages with said test scenario manager and to add simulation actions to said action queue.

18. (Original) A method as claimed in claim 16, wherein each signal interface controller includes a peripheral interface operable to transform simulation actions specified in said action queue into signal values exchanged with said hardware simulation.

19. (Original) A method as claimed in claim 11, wherein test scenario manager sends a machine generated sequence of simulation actions to said plurality of signal interface controllers to perform random simulation testing of said data processing apparatus.

20. (Original) A method as claimed in claim 11, wherein said test scenario manager is operable as a master device and said plurality of signal interface controllers are operable as slave devices to said master device.

21. (Currently Amended) A computer program product embodied on a computer-readable medium and comprising code that when executed controls a computer to simulate data processing operations performed by a data processing apparatus, said computer program product comprising:

hardware simulator code responsive to one or more stimulus signals to generate one or more response signals simulating a response of said data processing apparatus to said one or more stimulus signals if applied to said data processing apparatus;

a plurality of signal interface controller code blocks coupled to said hardware simulator code, each signal interface controller code block serving to perform one or more simulation actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of said hardware simulator code and said signal interface controller code block as part of simulating said data processing operations; and

test scenario manager code coupled to said plurality of signal interface controller code blocks and operable to transfer test scenario controlling messages to said plurality of signal interface controller code blocks, at least one of said test scenario controlling messages including:

(i) data defining a simulation action to be performed by a signal interface controller code block; and

(ii) data defining when said signal interface controller code block should perform said simulated action;; and

time generator code coupled to said plurality of signal interface controller blocks and said test scenario manager code for generating messages specifying time defining events corresponding to advancement of simulated time for said hardware simulatorcode,

wherein said test scenario manager code provides a shared data memory into which a signal interface controller code block may store data using a test scenario controlling message sent from said signal interface controller code block to said test scenario manager code, said data being readable from said shared data memory by another signal interface controller code block,

whereby said test scenario controlling messages are communicated via said shared data memory independently of advancement of simulated time by said messages specifying time defining events.

22. (Original) A computer program product as claimed in claim 21, wherein said data defining when said signal interface controller code block should perform said simulated action includes at least one of:

(i) a time value;

(ii) a delay value; and

(iii) a value specifying said simulated action should be performed when a specified event is simulated as occurring.

23. (Canceled).

24. (Previously Presented) A computer program product as claimed in claim 21, wherein a first signal interface controller code block is responsive to simulation results captured by a second signal interface controller code block, written to said shared data memory by said second signal interface controller code block and then read from said shared data memory by said first signal interface controller code block.

25. (Original) A computer program product as claimed in claim 21, wherein said hardware simulation is simulated using software running upon a general purpose computer.

26. (Original) A computer program product as claimed in claim 21, wherein each signal interface controller code block includes an action queue of simulation actions to be performed by said signal interface controller code block.

27. (Original) A computer program product as claimed in claim 26, wherein each signal interface controller code block includes a test scenario manager interface operable to exchange test scenario controlling messages with said test scenario manager code and to add simulation actions to said action queue.

28. (Original) A computer program product as claimed in claim 26, wherein each signal interface controller code block includes a peripheral interface operable to transform simulation actions specified in said action queue into signal values exchanged with said hardware simulation code.

29. (Original) A computer program product as claimed in claim 21, wherein test scenario manager code sends a machine generated sequence of simulation actions to said plurality of signal interface controller code blocks to perform random simulation testing of said data processing apparatus.

30. (Original) A computer program product as claimed in claim 21, wherein said test scenario manager code is operable as a master device and said plurality of signal interface controller code blocks are operable as slave devices to said master device.